3mA, 100MHz, 750V/µs Operational Amplifier with Shutdown

FEATURES

- **100MHz Gain Bandwidth**
- **750V/µs Slew Rate**
- **3.6mA Maximum Supply Current**
- **50µA Supply Current in Shutdown**
- 8nV/√Hz Input Noise Voltage
- Unity-Gain Stable
- 1.5mV Maximum Input Offset Voltage
- 4µA Maximum Input Bias Current
- 400nA Maximum Input Offset Current
- 40mA Minimum Output Current, V_{OUT} = ±3V
- ±3.5V Minimum Input CMR, V_S = ±5V
- 30ns Settling Time to 0.1%, 5V Step
- Specified at ±5V, Single 5V Supplies
- Operating Temperature Range: –40°C to 85°C

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

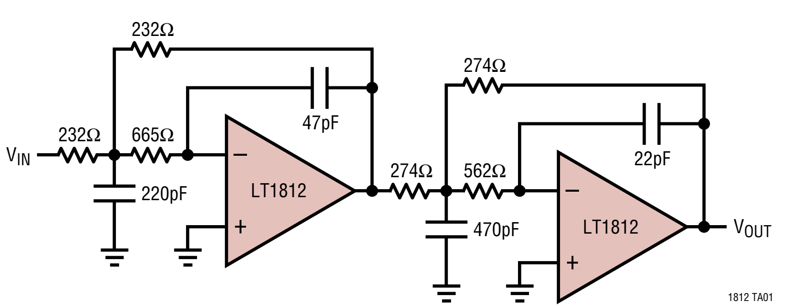
The LT®1812 is a low power, high speed, very high slew rate operational amplifier with excellent DC performance. The LT1812 features reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than other devices with comparable bandwidth. A power saving shutdown feature reduces supply current to 50µA. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier.

The output drives a 100Ω load to ±3.5V with ±5V supplies. On a single 5V supply, the output swings from 1.1V to 3.9V with a 100Ω load connected to 2.5V. The amplifier is stable with a 1000pF capacitive load which makes it useful in buffer and cable driver applications.

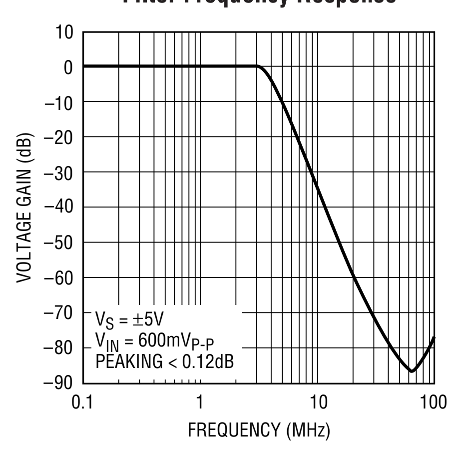
The LT1812 is manufactured on Linear Technology's advanced low voltage complementary bipolar process. The dual version is the LT1813. For higher supply voltage single, dual and quad operational amplifiers with up to 70MHz gain bandwidth, see the LT1351 through LT1365 data sheets.

TYPICAL APPLICATION

4MHz, 4th Order Butterworth Filter



Filter Frequency Response

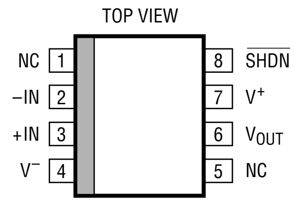


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Differential Input Voltage (Transient Only, Note 2) ... ±3V
Input Voltage .... $\pm V_S$
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 8) ... –40°C to 85°C
Specified Temperature Range
(Note 8) .... –40°C to 85°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 80°C/ W (NOTE 9)

ORDER PART NUMBER
LT1812CS8 LT1812IS8
S8 PART MARKING
1812 1812I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±5V, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)		0.4	1.5	mV
I_{OS}	Input Offset Current			30	400	nA
I_B	Input Bias Current			–0.9	±4	µA
e_n	Input Noise Voltage Density	f = 10kHz		8		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz		1		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = ±3.5V Differential	3	10 1.5		MΩ MΩ
C_{IN}	Input Capacitance			2		pF
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5	4.2 –4.2	 –3.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	75	85		dB
	Minimum Supply Voltage			±1.25	±2	V
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±5.5V	78	97		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω V_{OUT} = ±3V, R_L = 100Ω	1.5 1.0	3.0 2.5		V/mV V/mV
V_{OUT}	Maximum Output Swing	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive	±3.80 ±3.35	±4.0 ±3.5		V V
I_{OUT}	Maximum Output Current	V_{OUT} = ±3V, 30mV Overdrive	±40	±60		mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 1V Overdrive (Note 3)	±75	±110		mA
SR	Slew Rate	A_V = –1 (Note 5)	500	750		V/µs
FPBW	Full Power Bandwidth	3V Peak (Note 6)		40		MHz
GBW	Gain Bandwidth Product	f = 200kHz	75	100		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V, R_L = 100Ω		2		ns
OS	Overshoot	A_V = 1, 0.1V, R_L = 100Ω		25		%
t_{PD}	Propagation Delay	A_V = 1, 50% V_{IN} to 50% V_{OUT}, 0.1V, R_L = 100Ω		2.8		ns
t_s	Settling Time	5V Step, 0.1%, A_V = –1		30		ns
THD	Total Harmonic Distortion	f = 1MHz, V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 500Ω		–76		dB
	Differential Gain	V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 150Ω		0.12		%
	Differential Phase	V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 150Ω		0.07		DEG
R_{OUT}	Output Resistance	A_V = 1, f = 1MHz		0.4		Ω

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±5V$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN} > V^- + 2.0V$ (On) $\overline{SHDN} < V^- + 0.4V$ (Off)	 –100	0 –50	±1	µA µA
I_S	Supply Current	$\overline{SHDN} > V^- + 2.0V$ (On) $\overline{SHDN} < V^- + 0.4V$ (Off)		3 50	3.6 100	mA µA

$T_A = 25°C$, $V_S = 5V$, $V_{CM} = 2.5V$, R_L to 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)		0.5	2.0	mV
I_{OS}	Input Offset Current			30	400	nA
I_B	Input Bias Current			–1.0	±4	µA
e_n	Input Noise Voltage Density	f = 10kHz		8		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		1		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = 1.5V to 3.5V Differential	3	10 1.5		MΩ MΩ
C_{IN}	Input Capacitance			2		pF
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5	4 1	 1.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 3.5V	73	82		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω V_{OUT} = 1.5V to 3.5V, R_L = 100Ω	1.0 0.7	2.0 1.5		V/mV V/mV
V_{OUT}	Maximum Output Swing (Positive)	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive	3.9 3.7	4.1 3.9		V V
	Maximum Output Swing (Negative)	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive		0.9 1.1	1.1 1.3	V V
I_{OUT}	Maximum Output Current	V_{OUT} = 3.5V or 1.5V, 30mV Overdrive	±25	±40		mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 2.5V, 1V Overdrive (Note 3)	±55	±80		mA
SR	Slew Rate	A_V = –1 (Note 5)	200	350		V/µs
FPBW	Full Power Bandwidth	1V Peak (Note 6)		55		MHz
GBW	Gain Bandwidth Product	f = 200kHz	65	94		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V, R_L = 100Ω		2.1		ns
OS	Overshoot	A_V = 1, 0.1V, R_L = 100Ω		25		%
t_{PD}	Propagation Delay	A_V = 1, 50% V_{IN} to 50% V_{OUT}, 0.1V, R_L = 100Ω		3		ns
t_s	Settling Time	2V Step, 0.1%, A_V = –1		30		ns
THD	Total Harmonic Distortion	f = 1MHz, V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 500Ω		–75		dB
	Differential Gain	V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 150Ω		0.22		%
	Differential Phase	V_{OUT} = $2V_{P-P}$, A_V = 2, R_L = 150Ω		0.21		DEG
R_{OUT}	Output Resistance	A_V = 1, f = 1MHz		0.45		Ω
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN} > V^- + 2.0V$ (On) $\overline{SHDN} < V^- + 0.4V$ (Off)	 –50	0 –20	±1	µA µA
I_S	Supply Current	$\overline{SHDN} > V^- + 2.0V$ (On) $\overline{SHDN} < V^- + 0.4V$ (Off)		2.7 20	3.6 50	mA µA

$0°C \le T_A \le 70°C$, $V_S = ±5V$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			2	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7)		10	15	µV/°C
I_{OS}	Input Offset Current				500	nA
I_B	Input Bias Current				±5	µA

ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$. $V_S = \pm5V$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5		 −3.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm3.5V$	73			dB
	Minimum Supply Voltage				±2	V
PSRR	Power Supply Rejection Ratio	$V_S = \pm2V$ to $\pm5.5V$	76			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm3V$, $R_L = 500\Omega$ $V_{OUT} = \pm3V$, $R_L = 100\Omega$	1.0 0.7			V/mV V/mV
V_{OUT}	Maximum Output Swing	$R_L = 500\Omega$, 30mV Overdrive $R_L = 100\Omega$, 30mV Overdrive	±3.70 ±3.25			V V
I_{OUT}	Maximum Output Current	$V_{OUT} = \pm3V$, 30mV Overdrive	±35			mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0V$, 1V Overdrive (Note 3)	±60			mA
SR	Slew Rate	$A_V = -1$ (Note 5)	400			V/µs
GBW	Gain Bandwidth Product	f = 200kHz	65			MHz
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN} > V^- + 2.0V$ (On) $\overline{SHDN} < V^- + 0.4V$ (Off)	 −150		±1.5	µA µA
I_S	Supply Current	$\overline{SHDN} > V^- + 2.0V$ (On) $\overline{SHDN} < V^- + 0.4V$ (Off)			4.6 150	mA µA

$0°C \le T_A \le 70°C$, $V_S = 5V$, $V_{CM} = 2.5V$, R_L to 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			2.5	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7)		10	15	µV/°C
I_{OS}	Input Offset Current				500	nA
I_B	Input Bias Current				±5	µA
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5		 1.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1.5V$ to $3.5V$	71			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = 1.5V$ to $3.5V$, $R_L = 500\Omega$ $V_{OUT} = 1.5V$ to $3.5V$, $R_L = 100\Omega$	0.7 0.5			V/mV V/mV
V_{OUT}	Maximum Output Swing (Positive)	$R_L = 500\Omega$, 30mV Overdrive $R_L = 100\Omega$, 30mV Overdrive	3.8 3.6			V V
	Maximum Output Swing (Negative)	$R_L = 500\Omega$, 30mV Overdrive $R_L = 100\Omega$, 30mV Overdrive			1.2 1.4	V V
I_{OUT}	Maximum Output Current	$V_{OUT} = 3.5V$ or $1.5V$, 30mV Overdrive	±20			mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 2.5V$, 1V Overdrive (Note 3)	±45			mA
SR	Slew Rate	$A_V = -1$ (Note 5)	150			V/µs
GBW	Gain Bandwidth Product	f = 200kHz	55			MHz
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN} > V^- + 2.0V$ (On) $\overline{SHDN} < V^- + 0.4V$ (Off)	 −75		±1.5	µA µA
I_S	Supply Current	$\overline{SHDN} > V^- + 2.0V$ (On) $\overline{SHDN} < V^- + 0.4V$ (Off)			4.5 75	mA µA

$-40°C \le T_A \le 85°C$. $V_S = \pm5V$, $V_{CM} = 0V$ unless otherwise noted (Note 8).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			3	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7)		10	30	µV/°C
I_{OS}	Input Offset Current				600	nA
I_B	Input Bias Current				±6	µA
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5		 −3.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm3.5V$	72			dB

ELECTRICAL CHARACTERISTICS
$-40°C \le T_A \le 85°C$. $V_S = \pm5V$, $V_{CM} = 0V$ unless otherwise noted (Note 8).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Minimum Supply Voltage				±2	V
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±5.5V	75			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω V_{OUT} = ±3V, R_L = 100Ω	0.8 0.6			V/mV V/mV
V_{OUT}	Maximum Output Swing	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive	±3.60 ±3.15			V V
I_{OUT}	Maximum Output Current	V_{OUT} = ±3V, 30mV Overdrive	±30			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 1V Overdrive (Note 3)	±55			mA
SR	Slew Rate	A_V = –1 (Note 5)	350			V/µs
GBW	Gain Bandwidth Product	f = 200kHz	60			MHz
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ > V^- + 2.0V (On) $\overline{SHDN}$ < V^- + 0.4V (Off)	 –200		±2 	µA µA
I_S	Supply Current	$\overline{SHDN}$ > V^- + 2.0V (On) $\overline{SHDN}$ < V^- + 0.4V (Off)			5 200	mA µA

$-40°C \le T_A \le 85°C$, $V_S = 5V$, $V_{CM} = 2.5V$, R_L to 2.5V unless otherwise noted (Note 8).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			3.5	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7)		10	30	µV/°C
I_{OS}	Input Offset Current				600	nA
I_B	Input Bias Current				±6	µA
V_{CM}	Input Voltage Range (Positive) Input Voltage Range (Negative)		3.5 		 1.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 3.5V	70			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω V_{OUT} = 2.0V to 3.0V, R_L = 100Ω	0.6 0.4			V/mV V/mV
V_{OUT}	Maximum Output Swing (Positive)	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive	3.7 3.5			V V
	Maximum Output Swing (Negative)	R_L = 500Ω, 30mV Overdrive R_L = 100Ω, 30mV Overdrive			1.3 1.5	V V
I_{OUT}	Maximum Output Current	V_{OUT} = 3.5V or 1.5V, 30mV Overdrive	±17			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 2.5V, 1V Overdrive (Note 3)	±40			mA
SR	Slew Rate	A_V = –1 (Note 5)	125			V/µs
GBW	Gain Bandwidth Product	f = 200kHz	50			MHz
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ > V^- + 2.0V (On) $\overline{SHDN}$ < V^- + 0.4V (Off)	 –100		±2 	µA µA
I_S	Supply Current	$\overline{SHDN}$ > V^- + 2.0V (On) $\overline{SHDN}$ < V^- + 0.4V (Off)			5 100	mA µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Differential inputs of ±3V are appropriate for transient operation only, such as during slewing. Large sustained differential inputs can cause excessive power dissipation and may damage the part.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 5: Slew rate is measured between ±2V on the output with ±3V input for ±5V supplies and $2V_{P-P}$ on the output with a $3V_{P-P}$ input for single 5V supplies.

Note 6: Full power bandwidth is calculated from the slew rate:
$FPBW = SR/2\pi V_P$.

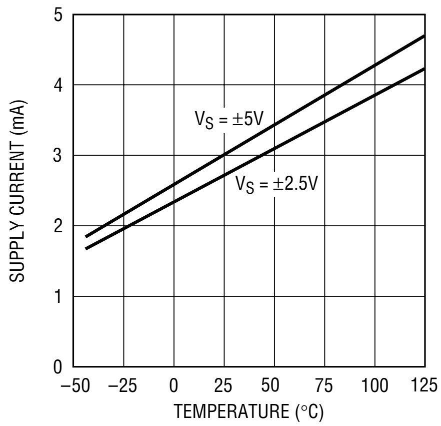
Note 7: This parameter is not 100% tested.

Note 8: The LT1812C is guaranteed to meet specified performance from 0°C to 70°C. The LT1812C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1812I is guaranteed to meet specified performance from –40°C to 85°C.

Note 9: θ_{JA} is specified for a $2500mm^2$ board covered with 2 oz copper on both sides. Thermal resistance varies, depending upon the amount of PC board metal attached to the device. For this package in particular, power is dissipated primarily through Pin 4, which should therefore, have a good thermal connection to a copper plane.

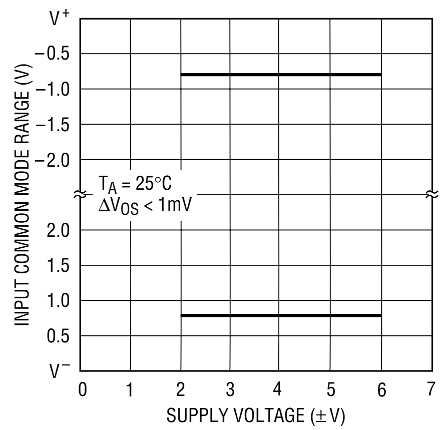
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



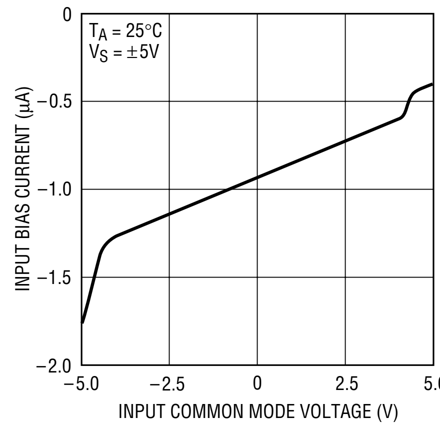
1812 G01

Input Common Mode Range vs Supply Voltage



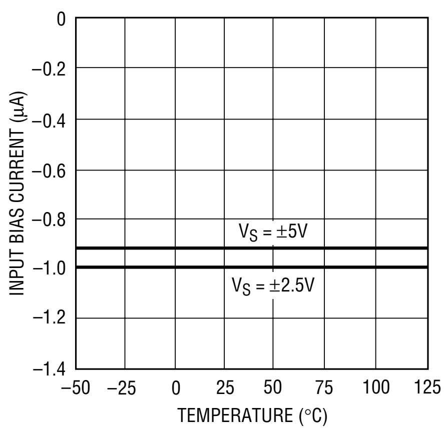
1812 G02

Input Bias Current vs Common Mode Voltage



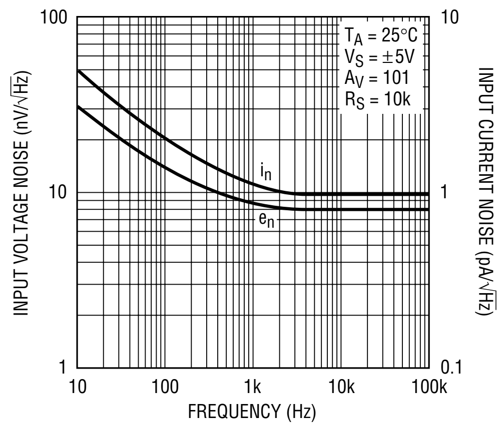
1812 G03

Input Bias Current vs Temperature



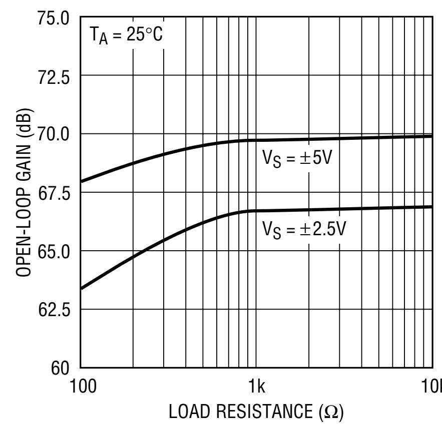
1812 G04

Input Noise Spectral Density



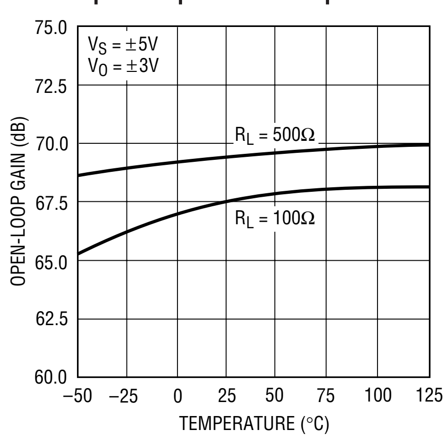
1812 G05

Open-Loop Gain vs Resistive Load



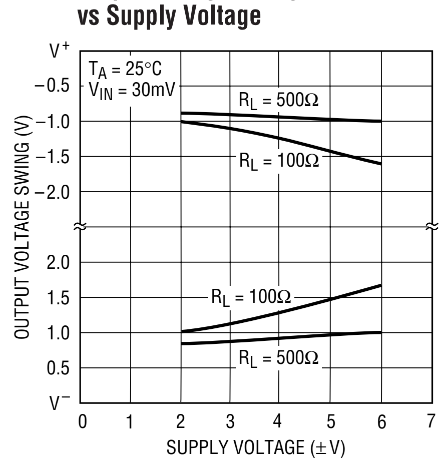
1812 G06

Open-Loop Gain vs Temperature



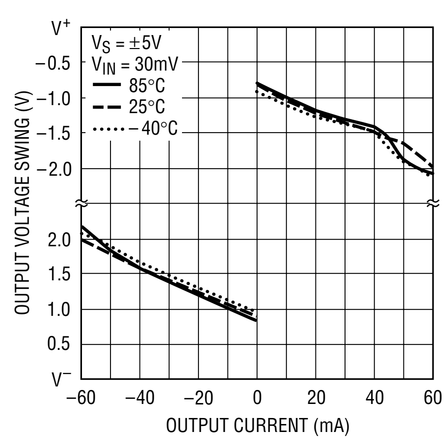
1812 G07

Output Voltage Swing vs Supply Voltage



1812 G08

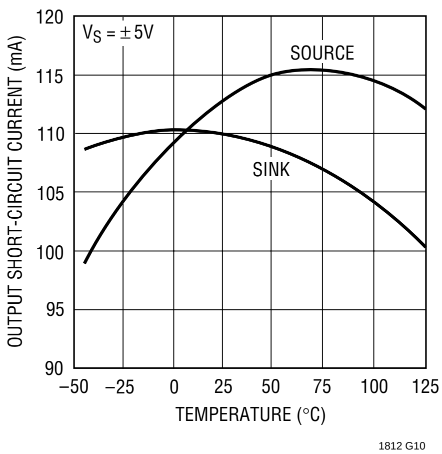
Output Voltage Swing vs Load Current



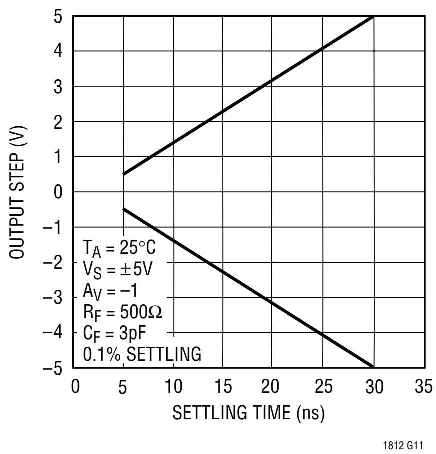
1812 G09

TYPICAL PERFORMANCE CHARACTERISTICS

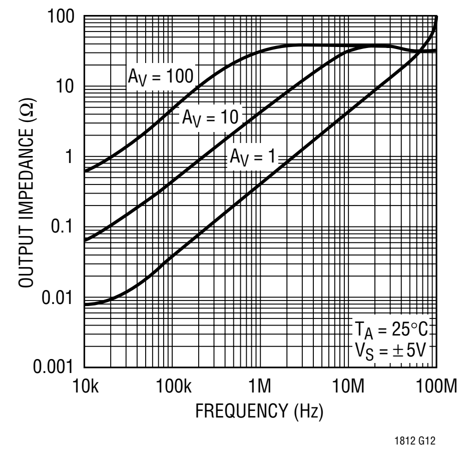
Output Short-Circuit Current vs Temperature



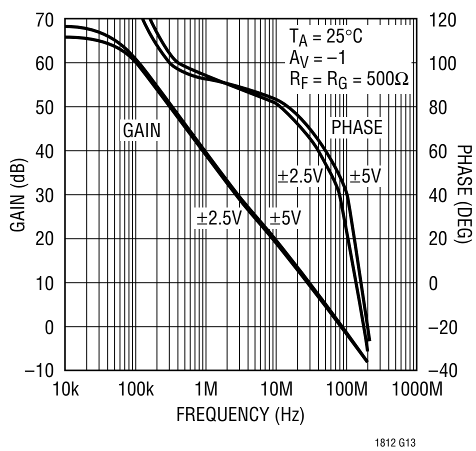
Settling Time vs Output Step



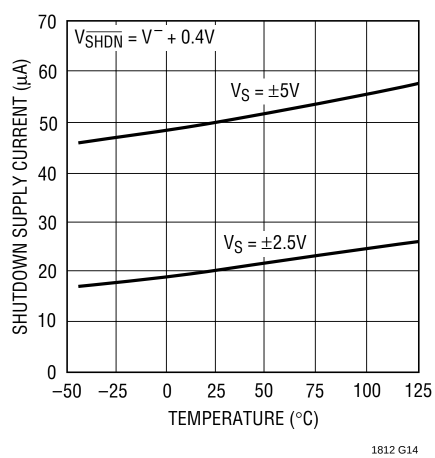
Output Impedance vs Frequency



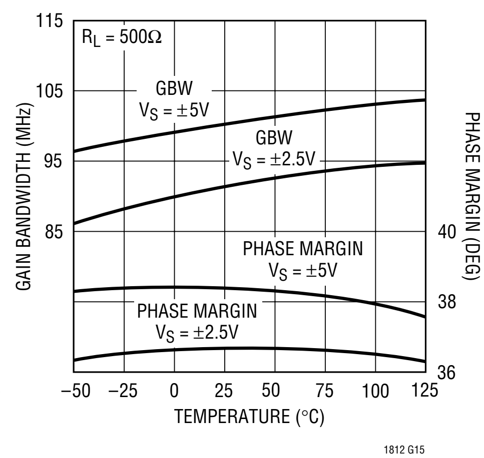
Gain and Phase vs Frequency



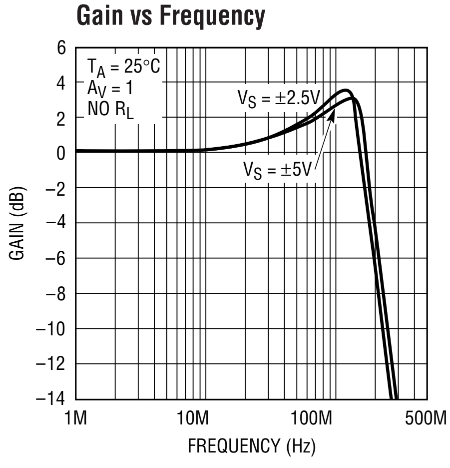
Shutdown Supply Current vs Temperature



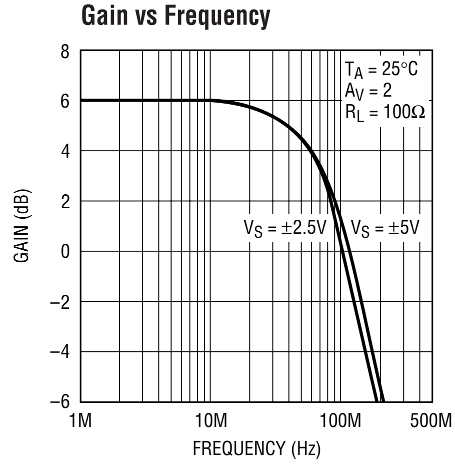
Gain Bandwidth and Phase Margin vs Temperature



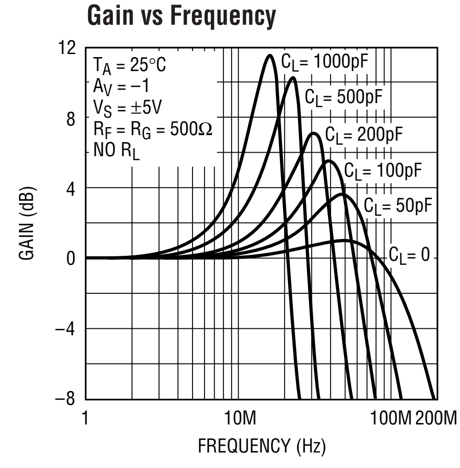
Gain vs Frequency



Gain vs Frequency

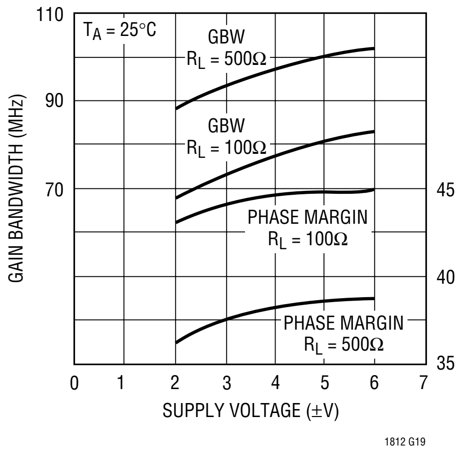


Gain vs Frequency

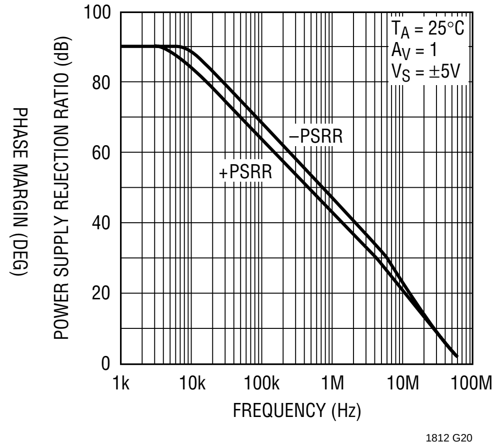


TYPICAL PERFORMANCE CHARACTERISTICS

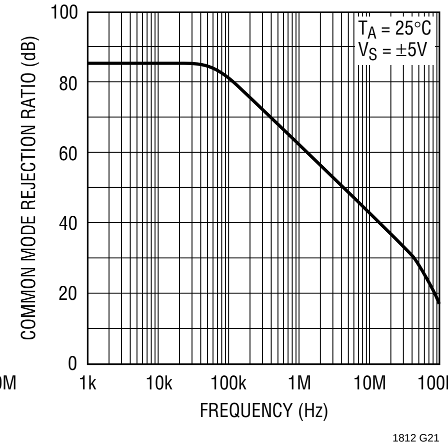
Gain Bandwidth and Phase Margin vs Supply Voltage



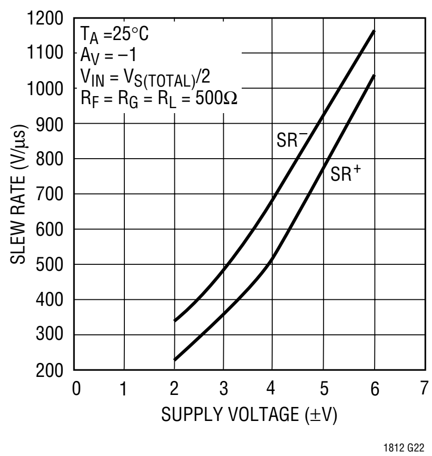
Power Supply Rejection Ratio vs Frequency



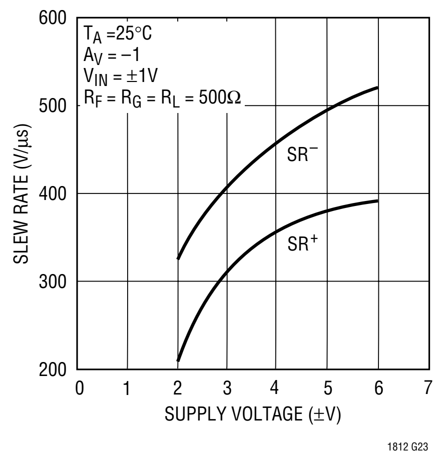
Common Mode Rejection Ratio vs Frequency



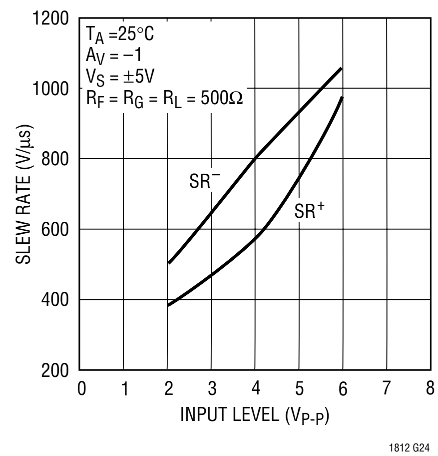
Slew Rate vs Supply Voltage



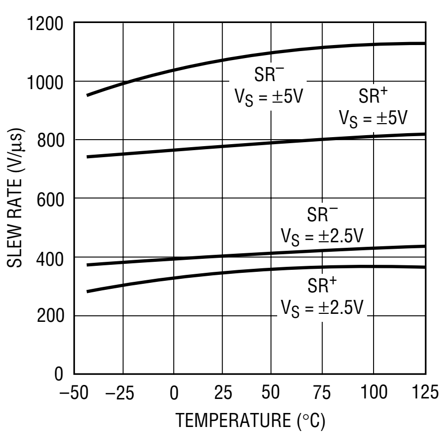
Slew Rate vs Supply Voltage



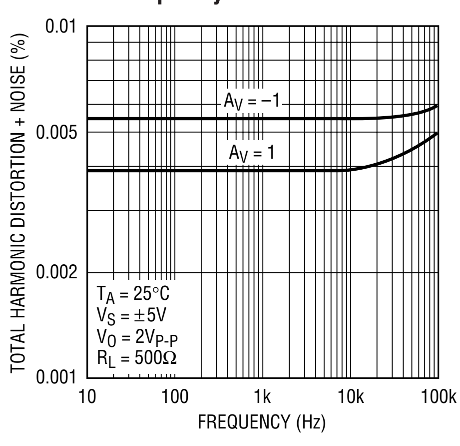
Slew Rate vs Input Level



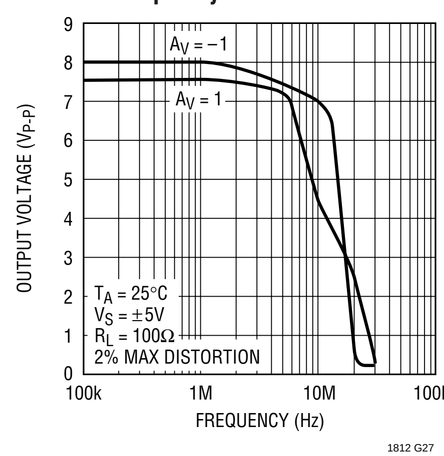
Slew Rate vs Temperature



Total Harmonic Distortion + Noise vs Frequency

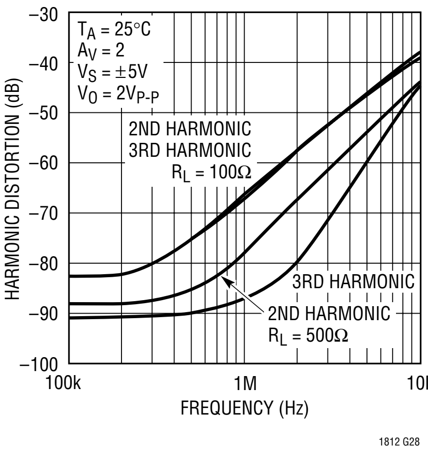


Undistorted Output Swing vs Frequency

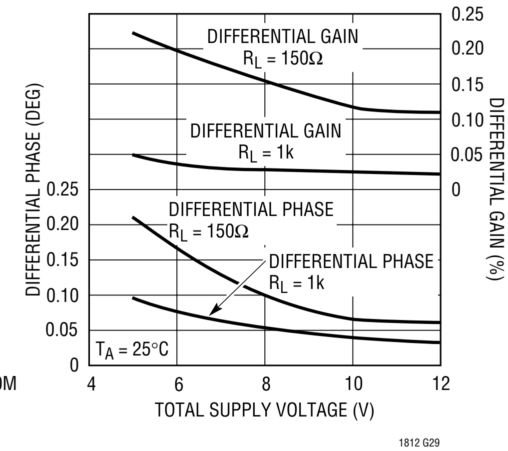


TYPICAL PERFORMANCE CHARACTERISTICS

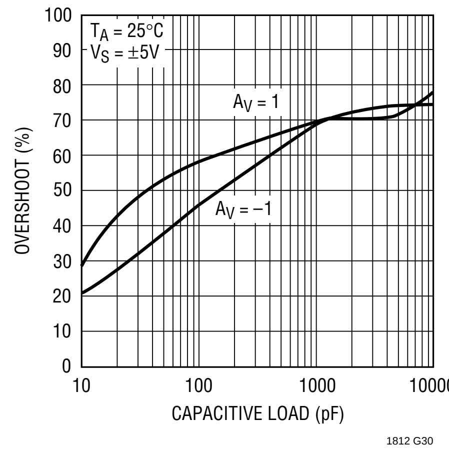
2nd and 3rd Harmonic Distortion vs Frequency



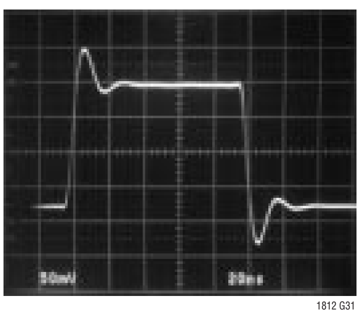
Differential Gain and Phase vs Supply Voltage



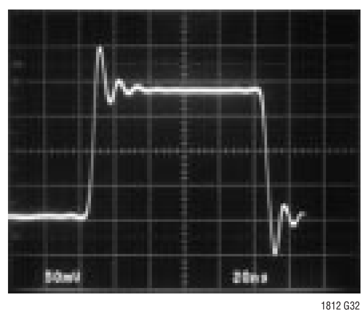
Capacitive Load Handling



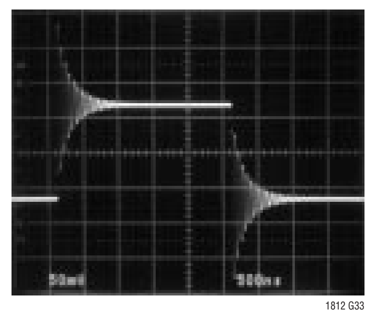
Small-Signal Transient, A_V = −1



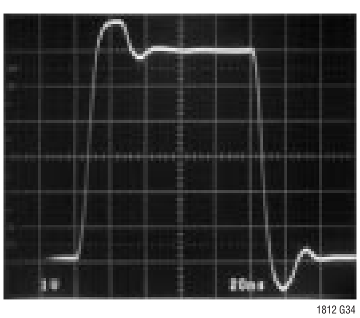
Small-Signal Transient, A_V = 1



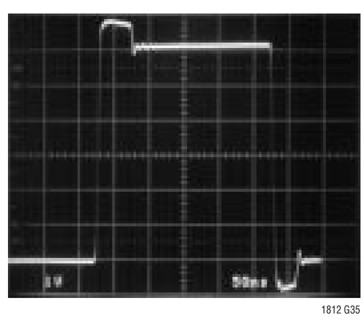
Small-Signal Transient, A_V = 1, C_L = 1000pF



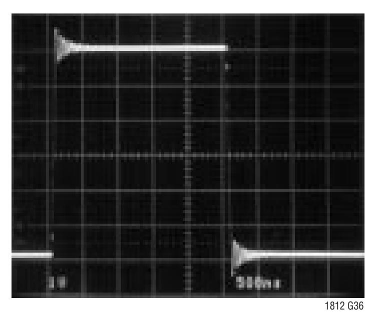
Large-Signal Transient, A_V = −1



Large-Signal Transient, A_V = 1



Large-Signal Transient, A_V = 1, C_L = 1000pF



APPLICATIONS INFORMATION

Layout and Passive Components

The LT1812 amplifier is more tolerant of less than ideal layouts than other high speed amplifiers. For maximum performance (for example, fast settling) use a ground plane, short lead lengths and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications, use low ESR bypass capacitors (1µF to 10µF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole that can cause peaking or even oscillations. If feedback resistors greater than 2k are used, a parallel capacitor of value

$$C_F > R_G \bullet C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is 1 and a large feedback resistor is used, C_F should be greater than or equal to C_{IN}. An example would be an I-to-V converter.

Input Considerations

Each of the LT1812 amplifier inputs is the base of an NPN and PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 3V without damage and need no clamping or source resistance for protection.

The device should not be used as a comparator because with sustained differential inputs, excessive power dissipation may result.

Capacitive Loading

The LT1812 is stable with a 1000pF capacitive load, which is outstanding for a 100MHz amplifier. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Coaxial cable can be driven directly, but for best pulse fidelity, a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Slew Rate

The slew rate is proportional to the differential input voltage. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 5V output step in a gain of 10 has a 0.5V input step, whereas in unity gain there is a 5V input step. The LT1812 is tested for slew rate in a gain of –1. Lower slew rates occur in higher gain configurations.

Shutdown

The LT1812 has a shutdown pin ($\overline{SHDN}$, Pin 8) for conserving power. When this pin is open or biased at least 2V above the negative supply, the part operates normally. When pulled down to V^-, the supply current drops to about 50µA. Typically, the turn-off delay is 1µs and the turn-on delay 0.5µs. The current out of the $\overline{SHDN}$ pin is also typically 50µA. In shutdown mode, the amplifier output is not isolated from the inputs, so the LT1812 shutdown feature cannot be used for multiplexing applications. The 50µA typical shutdown current is exclusive of any output (load) current. In order to prevent load current (and maximize the power savings), either the load needs to be disconnected, or the input signal needs to be 0V. Even in shutdown mode, the LT1812 can still drive significant current into a load. For example, in an $A_V = 1$ configuration, when driven with a 1V DC input, the LT1812 drives 2mA into a 100Ω load. It takes about 500µs for the load current to reach this value.

Power Dissipation

The LT1812 combines high speed and large output drive in a small package. It is possible to exceed the maximum junction temperature under certain conditions. Maximum

APPLICATIONS INFORMATION

junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1812CS8: $T_J = T_A + (P_D \bullet 80°C/W)$ (Note 9)

Power dissipation is composed of two parts. The first is due to the quiescent supply current and the second is due to on-chip dissipation caused by the load current. The worst-case load induced power occurs when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore P_{DMAX} is:

$P_{DMAX} = (V^+ – V^–)(I_{SMAX}) + (V^+/2)^2/R_L$ or

$P_{DMAX} = (V^+ – V^–)(I_{SMAX}) + (V^+ – V_{OMAX})(V_{OMAX}/R_L)$

Example: LT1812CS8 at 70°C, $V_S = \pm5V$, $R_L = 100\Omega$

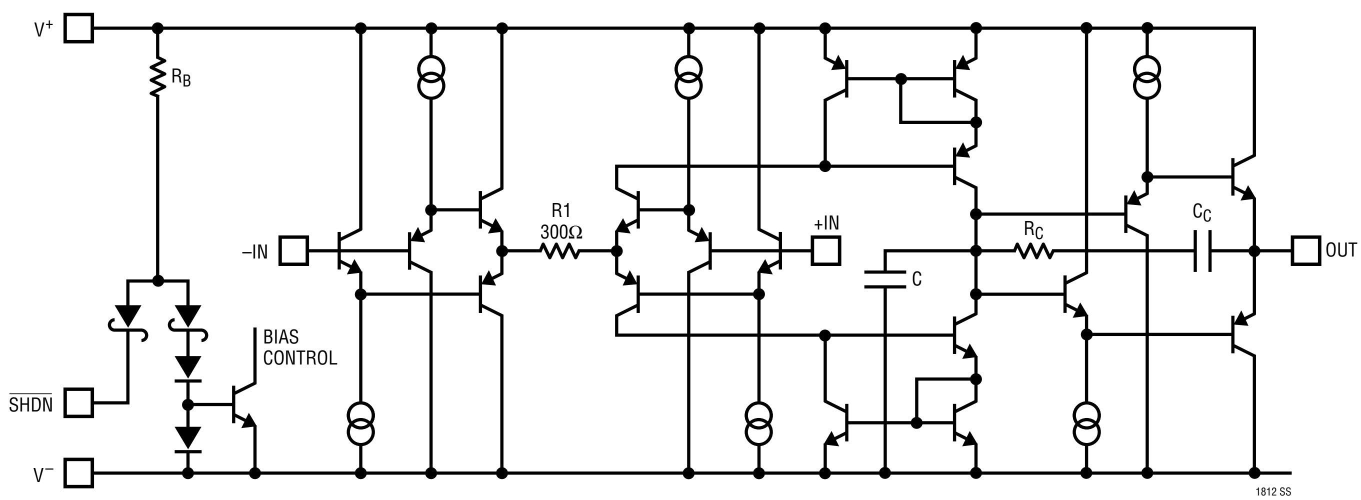
$P_{DMAX} = (10V)(4.5mA) + (2.5V)^2/100\Omega = 108mW$

$T_{JMAX} = 70°C + (108mW)(80°C/W) = 79°C$

Circuit Operation

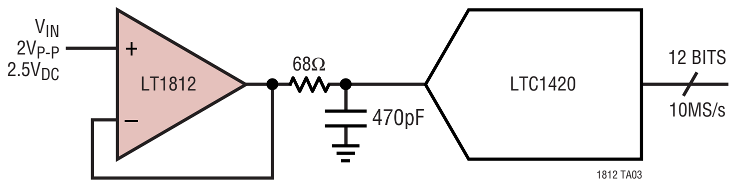
The LT1812 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic. The inputs are buffered by complementary NPN and PNP emitter followers that drive a 300Ω resistor. The input voltage appears across the resistor generating currents that are mirrored into the high impedance node. Complementary followers form an output stage that buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving capacitive loads (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain cross away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that the total phase lag does not exceed 180 degrees (zero phase margin) and the amplifier remains stable. In this way, the LT1812 is stable with up to 1000pF capacitive loads in unity gain, and even higher capacitive loads in higher closed-loop gain configurations.

SIMPLIFIED SCHEMATIC



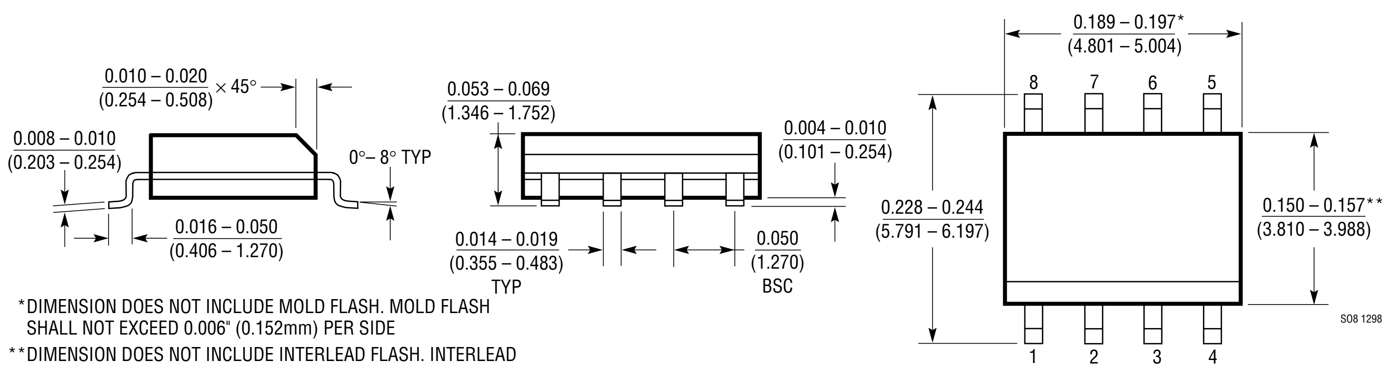
TYPICAL APPLICATION

Single 5V Supply 10MS/s 12-Bit ADC Buffer



PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1360/LT1361/LT1362	Single/Dual/Quad 50MHz, 800V/µs, C-Load™ Amplifiers	4mA Supply Current, 1mV Max V_{OS}, 1µA Max I_B
LT1363/LT1364/LT1365	Single/Dual/Quad 70MHz, 1000V/µs C-Load Amplifiers	50mA Output Current, 1.5mV Max V_{OS}, 2µA Max I_B
LT1395/LT1396/LT1397	Single/Dual/Quad 400MHz Current Feedback Amplifiers	4.6mA Supply Current, 800V/µs, 80mA Output Current
LT1398/LT1399	Dual/Triple 300MHz Current Feedback Amplifiers	4.5mA Supply Current, 80mA Output Current, Shutdown
LT1813	Dual 3mA, 100MHz, 750V/µs Operational Amplifier	Dual Version of the LT1812

C-Load is a trademark of Linear Technology Corporation.

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1812f LT/TP 0200 4K • PRINTED IN USA